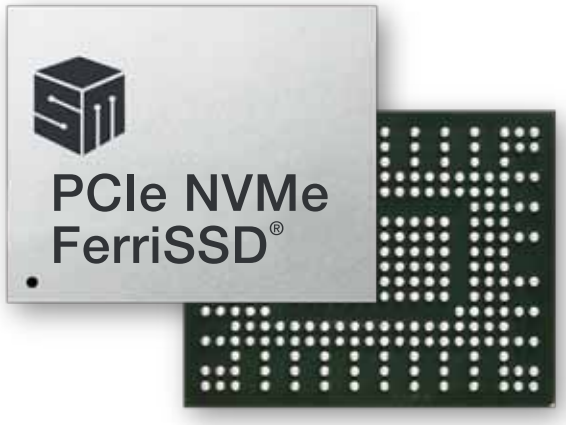
SiliconMotion

WHITE PAPER

Silicon Motion's PCIe FerriSSD®

Designed Specifically for Industrial / Embedded Applications

The increasing popularity of cloud computing systems, and in particular the Internet of Things (IoT), means that demand is growing rapidly for reliable access to data at ever higher data-transfer rates. This increase in demand for data applies equally to storage: as a result the PCIe/NVME SSD, which has a very high-speed interface to support fast Read and Write operations, is rapidly becoming the preferred solution for data storage in many IoT applications.



For industrial and embedded systems, the primary requirement for data storage, as for any other important system function, is very high reliability. But in the embedded world too, speed and performance are also crucial parameters. The PCIe/NVME SSD has the potential to satisfy both requirements. The high-speed PCIe/NVME interface can help improve application performance so that an embedded system can process more instructions and answer more complex queries in less time. In embedded systems, I/O-intensive log files and frequently accessed tables can slow down an analytics engine, but a PCIe-based Flash storage unit keeps the data near to the processor, providing a fast response time to requests for data.

The ability to access data quickly is, of course, of little value if the data has been corrupted or lost. The reliability of data storage may be compromised in many ways, such as power failure, memory failure, system instability and even human error. This is why manufacturers of NAND Flash-based storage systems have developed special technologies for data protection, to avoid the risk of system faults or even total failure caused by corruption or loss of stored data.

The development of data protection and data integrity technology has reached a new level with the introduction of the PCIe FerriSSD®, a NAND Flash-based data storage solution from Silicon Motion which is ideal for a wide range of embedded applications requiring fast access speed, a small flexible form factor and a reliable boot and storage drive.

In order to meet demanding boot load SSD performance specifications and to provide robust data protection, the new PCIe FerriSSD incorporates various unique technologies which enhance the data integrity, longevity and performance of SSD boot loaders, including:

- **DRAM cache with data redundancy**
- **Full end-to-end data path protection**
- **IntelligentScan & DataRefresh**
- **Hybrid Zone**

DRAM cache with data redundancy: no data loss during data transfers

Silicon Motion's new PCIe FerriSSD features an embedded DRAM which has a self-error detection and correction code (ECC) capability. This DRAM provides for secure, frequent read/write cache requests, and stores logical-to-physical address mapping information.

When the PCIe FerriSSD communicates with the host system and data is written to or read from the NAND Flash memory array, the DRAM temporarily stores the internal Flash mapping tables, as well as the user data that is being written or read.

This provides insurance in case a sudden defect occurs in the NAND Flash storage medium during the data programming process: the PCIe FerriSSD can use the redundant data in the DRAM to complete the data programming process to the NAND Flash array without delay to the host, eliminating the risk of data loss during any transfer of data between NAND Flash and host.

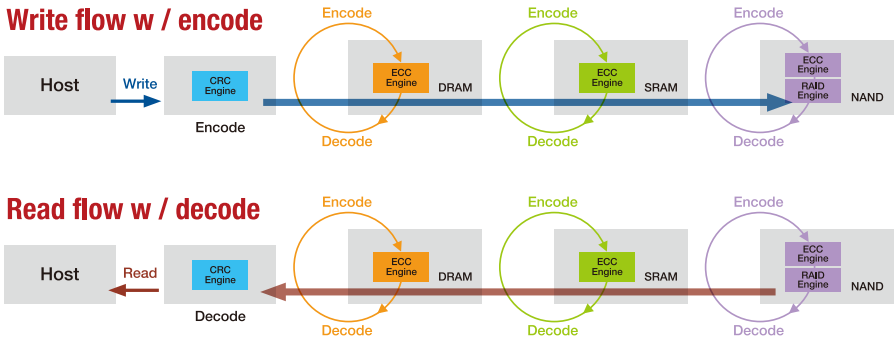
Full end-to-end data path protection: no bit errors sent to host

Conventional SSDs may employ error detection and correction circuitry at the far ends of the data path: at the front-end host interface and at the back-end NAND interface. This omits an important gap at the internal SRAM and/or DRAM transfer buffers, and other circuit paths. Data errors that occur between the NAND interface and the host, such as soft error bits, are often extremely difficult to identify and duplicate.

While conventional SSDs may have some internal error detection circuitry, the new PCIe FerriSSD storage solutions incorporate full data recovery engines to provide enhanced data integrity throughout the entire Host-to-NAND-to-Host data path.

The PCIe FerriSSD data recovery algorithm can effectively detect any error in the SSD data path, including hardware errors, firmware errors and memory errors arising in SRAM, DRAM or NAND. The PCIe FerriSSD implements an additional redundant back-up in NAND – the SMI Ferri Group Page Raid – which reinforces the protection against the risk of uncorrectable error in the NAND storage medium.

Should the PCIe FerriSSD identify any error that cannot be self-corrected, it will pass an error flag to the host for appropriate recovery processing. By contrast, conventional SSDs pass faulty data to the host without an error flag, exacerbating the initial problem by failing to alert the host to the need for error recovery processing.



end-to-end data path protection
- Whole SSD error Detection
- DRAM error Detection with Correction
- SRAM error Detection with Correction
- NAND Flash ECC Detection with Correction
  - Hard-decode (BCH)
  - Soft-decode (LDPC)
  - Group page RAID

No error data will be sent to host!

IntelligentScan & DataRefresh: proactive data loss prevention measures

The features described above protect against the risk of data loss or error in data-transfer operations. The PCIe FerriSSD also incorporates sophisticated functions which ensure the integrity of data in storage.

The IntelligentScan & DataRefresh function achieves this by identifying at-risk memory cells and refreshing the data stored in them. The risk of loss of stored data increases as:

- **the aggregate number of Program / Erase (P/E) cycles increases**
- **the ambient temperature rises**

In either condition, the operation of the IntelligentScan & DataRefresh function becomes increasingly important.

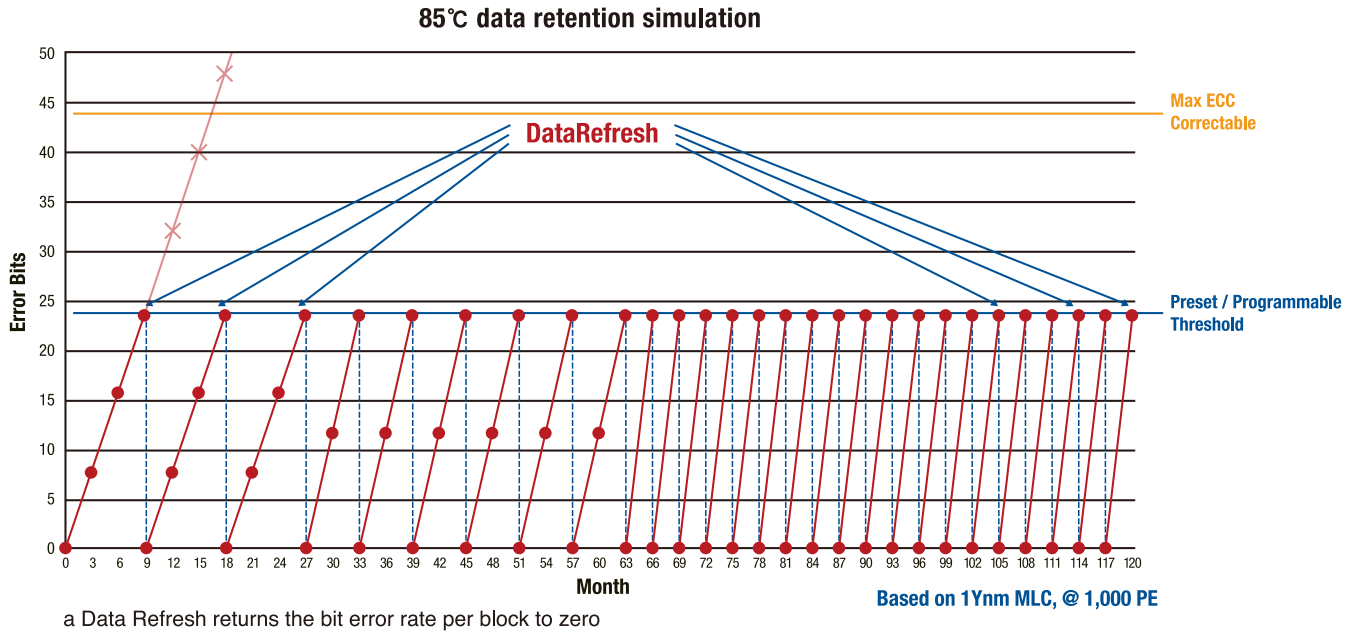
Effect of temperature on data retention

One of the most significant inhibitors to data retention is elevated NAND temperature – the higher the ambient working temperature, the shorter the retention capability of the NAND itself. The PCIe FerriSSD incorporates a Silicon Motion patent-pending monitoring algorithm which logs cumulative junction temperature readings, the number of P/E cycles, SSD power on-time, and other essential reference points to dynamically select and prioritize which NAND cells to DataRefresh, and when.

IntelligentScan & DataRefresh work together to significantly extend the retention capability at various temperatures before data becomes unrecoverable.

Thermo impact on NAND Data Retention

Temp	SLC @ max PE	MLC @ max PE
40	75.58 Mo	12 Mo
55	12 Mo	1.88 Mo
70	2.14 Mo	0.34 Mo
85	0.45 Mo	0.07 Mo



a Data Refresh returns the bit error rate per block to zero

Read disturbance

Performing an excessive number of read cycles from a cell, can cause unintended over-charging of adjacent cells, leading to unrecoverable bit errors, a phenomenon known as Read disturbance. FerriSSD products avoid potential Read disturbance errors by performing periodic IntelligentScan & DataRefresh operations on NAND blocks that undergo repetitive Read cycles. The PCIe FerriSSD firmware – an advanced 4th generation algorithm (IntelligentScan) – automatically manages DataRefresh cycles and processing time to minimize data loss due to the impact of intensive Read operations on the NAND Flash storage medium.

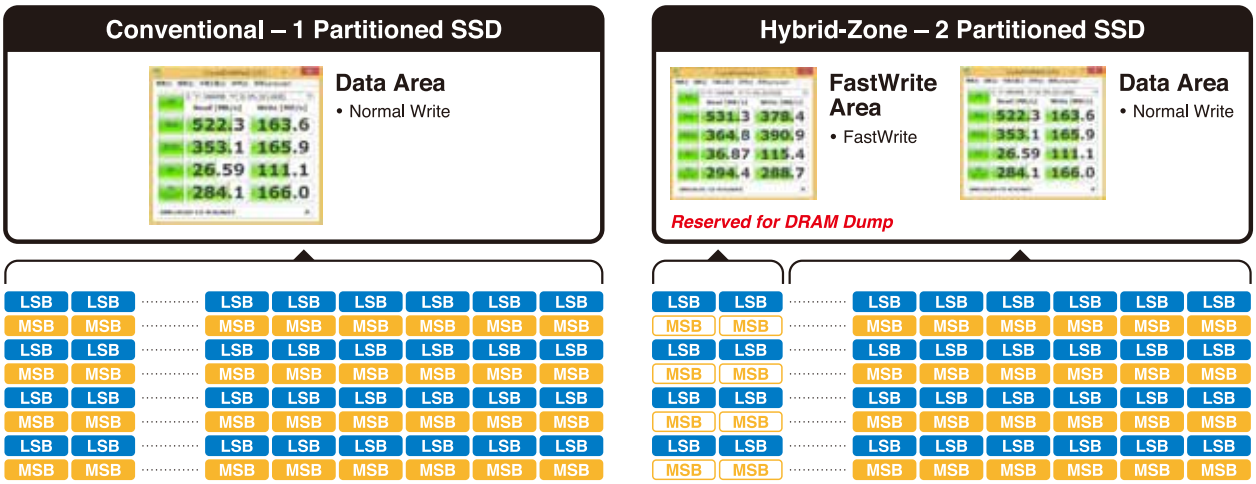
Hybrid Zone:
ideal blend of cost, reliability and performance

In conventional SSDs, the NAND dies of which the memory array is composed are configured as single-layer cells (SLC), multi-layer cells (MLC), or the new 3D triple-layer cells (TLC). The selection of SLC vs. MLC vs. TLC is made to achieve the best trade-off between memory density and access latency: SLC offers the lowest latency and density, and TLC the highest memory density, but also the highest latency. MLC cells fall somewhere between SLC and TLC on both counts.

Hybrid Zone, a unique feature of the PCIe FerriSSD, offers a way to take advantage both of the low latency of SLC cells and the high memory density of TLC cells.

The Hybrid Zone feature partitions a single NAND die into separate SLC and MLC/TLC zones. Partitioning a single drive is particularly useful in low- to medium-density SSDs.

Without foregoing the density benefits of MLC/TLC, single NAND die SSDs can still maintain fast Write SLC memory, which is ideal for emergency power shutdown operations. Without a portion of memory implemented as SLC, both the cost and the size of battery storage needed for MLC/TLC power shutdown would increase. The implementation of SLC memory is also ideal for high reliability and fast access—assigning SLC to boot code for instance – while also preserving a portion of the NAND medium for higher density MLC/TLC uses.



Conclusion

The latest generation of embedded and industrial applications rely heavily on faster data transfer rates, and robust and reliable data storage. The migration to PCIe SSDs provides a proven way to achieve the required performance in embedded storage applications.

The new PCIe FerriSSD from Silicon Motion offers not only improved performance: advanced technologies such as embedded DRAM data redundancy protect the SSD from the risk of data loss during data transfer operations.

Available in 3D TLC, MLCand SLC modes, and with memory capacity options ranging from 4GB to 256GB, FerriSSD provides great flexibility to system designers, allowing them to match the specification of their storage solution to the needs of their application, and thus to minimize the cost of the SSD. For many embedded applications, the improved performance and added data protection in the new PCIe FerriSSD will make it the right choice.

Silicon Motion's engineers have developed a full array of advanced technologies to prolong the life of the SSD, including a proven 4th generation data recovery algorithm. The new PCIe FerriSSD offers the best blend of data integrity, cost and performance for embedded and industrial applications.